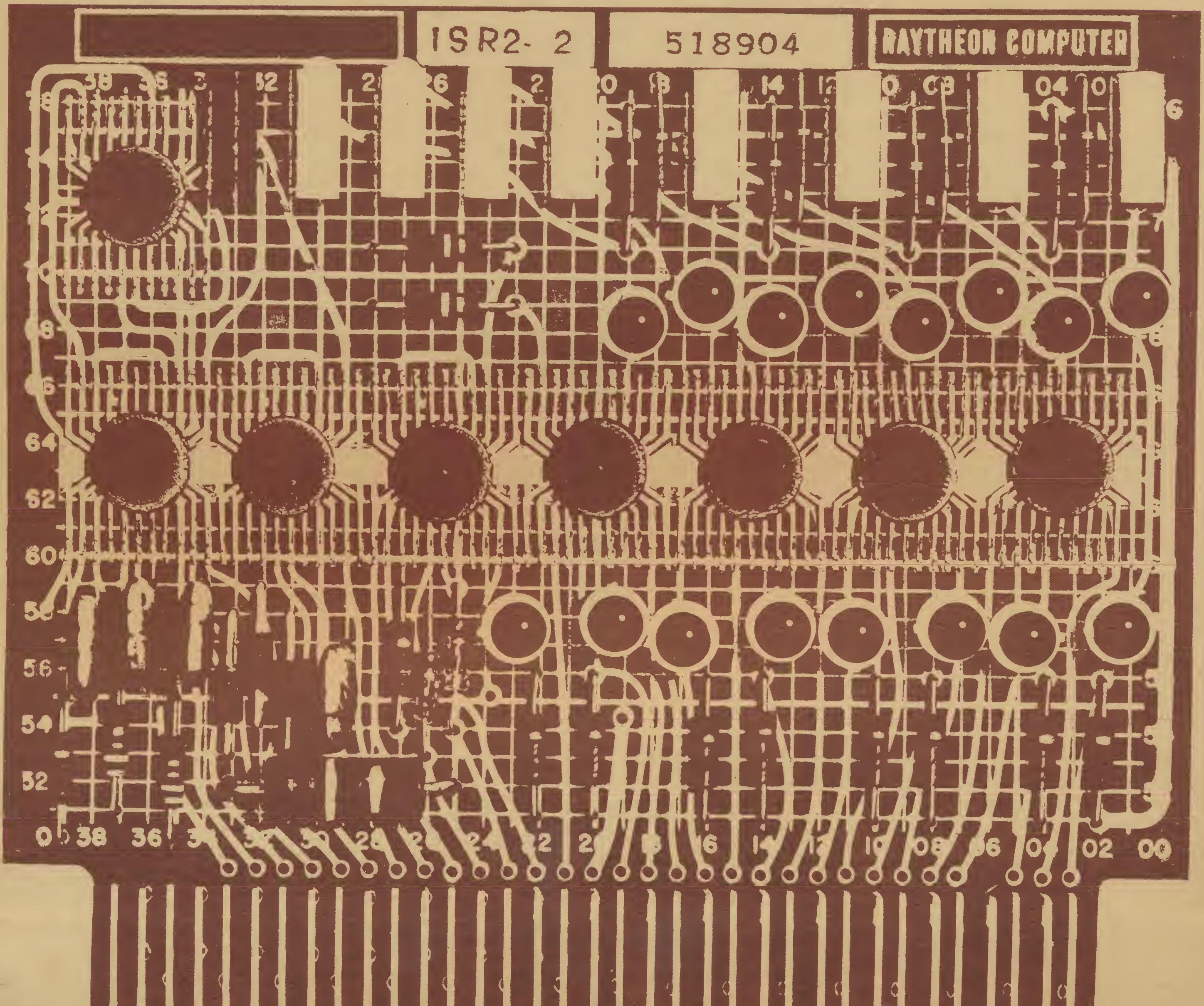
SP-206

Integrated Circuit Digital Modules with the Highest Guaranteed Noise Rejection:

1.5 Volts on Clock Lines

30 Volts on Data Lines

and that's not just a lot of noise from Raytheon Computer



Raytheon Computer "I" Series Integrated Circuit Modules Are Compatible With These Standard Raytheon Computer "G" Series Modules

MODULE	200KC	1MC	5MC	20MC
Amplifier Inverter, 12 circuits	GAI2-.2	GAI2-1	—	—
Amplifier Inverter, 4 circuits	—	—	—	GAI3-20
Binary Counter, 4 circuits	GBC1-.2	GBC1-1	GBC1-5	—
Clock Generator, free running	GCG1-.2	GCG1-1	GCG1-5	—
Clock Generator, crystal controlled 40kc to 200kc	GCG2-.2	GCG2-1	GCG2-5	—
Decade Counter, 8-4-2-1 Code out	GDC1-.2	GDC1-1	GDC1-5	—
Diode AND Gate, 20 inputs, 6 outputs	—	GDG2-1	GDG2-5	—
Diode OR Gate, 21 inputs, 5 outputs, level restoring	GDG3-.2	GDG3-1	GDG3-5	—
AND Gate, 3 input, 4 circuits	—	—	—	GDG4-20
OR Gate, 3 input, 4 circuits	—	—	—	GDG5-20
Driver Inverter, 10 circuits	GDI1-.2	GDI1-1	GDI1-5	—
Driver Inverter, 10 circuits, cable driver	GDI2-.2	GDI2-1	GDI2-5	—
Delay Line, Magnetostrictive, to 1300 μ sec.	—	GDL1-1	—	—
Decoder Matrix—Binary to octal or 16 line	—	GDM1-1	GDM1-5	—
Data Receiver, 3 circuits	GDR1-.2	—	—	—
Emitter Follower, 12 circuits	GEF1-.2	GEF1-1	GEF1-5	—
Flip-flop, 4 circuits, universal	GFF1-.2	GFF1-1	GFF1-5	—
Flip-flop, RS, 4 circuits	GFF2-.2	GFF2-1	GFF2-5	—
Flip-flop, Gated, 4 circuits	GFF3-.2	GFF3-1	GFF3-5	—
Flip-flop, Gated, 2 circuits	—	—	—	GFF4-20
Half Adder, Subtractor, Comparator, 4 circuits	GHA1-.2	GHA1-1	GHA1-5	—
Input Gate, Pulse OR Gate, 22 inputs, 10 outputs	GIG1-.2	GIG1-1	GIG1-5	—
Linear Amplifier, Gain 90, 20 cps to 1 MC, 2 circuits	—	GLA1-1	—	—
Level Converter, 7090 to RC-9 circuits	GLC1-.2	—	—	—
Level Converter, RC to 7090—4 circuits	GLC2-.2	—	—	—
Level Converter, RC to IBM current mode P-8 circuits	GLC3-.2	—	—	—
Level Converter, RC to IBM current mode N-8 circuits	GLC4-.2	—	—	—
Level Converter, IBM current mode N to RC-8 circuits	GLC5-.2	—	—	—
Level Converter, IBM current mode P to RC-8 circuits	GLC6-.2	—	—	—
Level Converter, RC to IBM current mode C level, 8 circuits	—	GLC7-1	—	—
Level Converter, IBM mode C levels to RC, 8 circuits	—	GLC8-1	—	—
Level Converter, 0 and —2v. to RC, 12 circuits	GLC9-.2	GLC9-1	GLC9-5	—
Multivibrator Clock, with 2 gated drivers	GMV1-.2	GMV1-1	—	—
NAND Gate, 16 inputs, 6 outputs	GNA1-.2	GNA1-1	GNA1-5	—
One-Shot, 3 circuits	GOS3-.2	GOS3-1	GOS3-5	—
Reset Gate, 4 circuits, 6 outputs per circuit	GRG1-.2	GRG1-1	GRG1-5	—
Bidirectional Shift Register, 2 circuits	GSR2-.2	GSR2-1	GSR2-5	—
Bidirectional Shift Register, 3 circuits	GSR3-.2	GSR3-1	GSR3-5	—
Shift Register, Serial, Parallel, 4 circuits	GSR4-.2	GSR4-1	GSR4-5	—
Schmitt Trigger, 4 circuits	GST1-.2	GST1-1	GST1-5	—
Schmitt Trigger, 2 circuits, adjustable threshold	GST2-.2	GST2-1	GST2-5	—
Universal Logic, 18 Gate inputs, 4 inverters	GUL1-.2	GUL1-1	GUL1-5	—

ANALOG MODULES

Digital-to-Analog Converter 8 bits or 2 4-bits Binary or BCD Bipolar or Unipolar	GDA1
Digital-to-Analog Converter, 10 bits Binary	GDA2
Reference Voltage Supply Module,–5 v.	GRS1
Voltage Comparator	GVC1

SPECIAL MODULES

Display Driver, 6 circuits, ½ Binary to Decimal	GDD1
Nixie Driver, 8-4-2-1 and complement code input	GND1
Relay or Lamp Driver, 8 circuits, 350 ma, —48v.	GPA1
Power Amplifier, 12 circuits, 150 ma, 28v.	GPA2
Reed Relay, 4 relays with drivers	GRR1
Reed Relay, 8 relays with drivers	GRR2
Silicon Switch, 4 SCR, 200 ma, 100v.	GSS1

Technical representatives and company sales offices:

Alabama, Fact-Tronics, P.O. Box 1135, Huntsville, (205) 539-7193; Raytheon Computer, Holiday Office Center, Suite 47, Huntsville, (205) 881-2844; **Arizona,** Barnhill Assoc., 30 Pima Plaza, Office 20, Scottsdale, (602) 947-5493; **California,** Dynamic Assoc., Inc., 1011-D Industrial Way, Burlingame, (415) 344-2521; Raytheon Computer, 2700 South Fairview Street, Santa Ana, (714) 546-7160; Williams & Hedge, Inc., 4341 West Commonwealth, Fullerton, (714) 521-7410; **Colorado,** Barnhill Assoc., 1170 So. Sheridan Blvd., Denver, (303) 934-5505; **Connecticut,** Eltron Engr. Sales, 2341 Whitney Avenue, Hamden, (203) AT 8-9276; **Florida,** Fact-Tronics, P.O. Box 3202, Orlando, (305) GA 3-7069; **Georgia,** Fact-Tronics, 254 East Paces Ferry Road, Atlanta, (205) WX-4000; **Illinois,** Pivan Engineering, 3535 West Peterson Avenue, Chicago, (312) KE 9-4838; **Indiana,** Pivan Engineering, 10447 North College Avenue, Indianapolis, (317) VI 6-5805; **Iowa,** Pivan Engineering, P.O. Box 851, Cedar Rapids, (319) 365-6635; **Maryland,** L. G. White & Co., 880 Bonifant Street, Silver Spring, (301) JU 5-3141; **Massachusetts,** Eltron Engr. Sales, 246 Walnut Street, Newtonville, (617) DE 2-6975; **Michigan,** WKM Associates, Inc., 19430 Mount Elliott, Detroit, (313) 366-0840; **Minnesota,** Pivan Engineering, P.O. Box 387, Osseo, (612) 335-3333; **New Jersey & Met. New York,** Kenneth E. Hughes Co., Inc., 4808 Bergenline Avenue, Union City, (201) UN 7-3204; **New York,** D. B. Associates, Inc., 3307 Erie Blvd. East, DeWitt, (315) 446-0220; D. B. Associates, Inc., 22 Biscayne Drive, Lancaster, (716) TF 5-6186; Raytheon Computer, 1501 Franklin Avenue, Mineola, L.I., (516) PI 7-3705; **New Mexico,** Barnhill Assoc., 319A Wyoming, N.E., Albuquerque, (505) 265-7766; **North Carolina,** L. G. White & Co., P.O. Box 2356, Winston-Salem, (919) 725-3612; **Ohio,** WKM Associates, Inc., 6741 Ridge Road, Cleveland, (216) 885-5616; WKM Associates, Inc., 6085 Far Hills Avenue, Dayton, (513) 298-7203; **Pennsylvania,** L. G. White & Co., 100 Essex Ave., North, Narbeth, (215) MO 4-6505; WKM Associates, Inc., 90 Clariton Blvd., Pittsburgh, (412) 892-2953; **Texas,** Raytheon Computer, 204 East Main, Arlington, (817) CR 5-5361; J. Y. Schoonmaker Co., Inc., 5328 Redfield Avenue, Dallas, (214) ME 1-8480; **Washington,** The Thorson Co., 1767 15th Avenue, So., Seattle, (206) EA 5-5000; **Washington, D.C.** Raytheon Computer, 4217 Wheeler Ave., Alexandria, Virginia, (703) 836-7616; **Canada,** Radionics Limited, 8230 Mayrand Street, Montreal 9, Quebec, REgent 9-5517; Radionics Limited, 4938 Yonge Avenue, Willowdale, Ontario.

RAYTHEON

Raytheon Computer, 2700 South Fairview Street, Santa Ana, California 92704

Raytheon Computer Integrated Circuit Modules

Why buy integrated circuit modules with inadequate protection against noise? Raytheon Computer now offers silicon IC digital modules that are virtually impervious to system noise. These new ICs give you 1.5 volts guaranteed noise rejection on clock lines, 30 volts on data lines. And buffering provides 3 volt rejection on all outputs. The new IC modules operate at 200KC and are compatible with the more than 100 existing Raytheon Computer discrete component digital modules for 200KC, 1MC, 5MC and 20MC frequencies. This means you can buy our lower-priced 200KC IC modules and not give up high frequency capability. Raytheon IC modules are on the same compact 3¾″ x 4¼″ 35-pin boards as the discrete units and have compatible logic levels and power requirements. IC flatpacks are mounted with parallel gap soldering, resulting in smaller, stronger joints which make encapsulation unnecessary. Logic density is as high as 28-flip-flops per board.

NOISE REJECTION Raytheon Computer "I" series modules using advanced circuit techniques offer extremely high noise rejection. The "I" series modules are virtually impervious to system noise. Data is entered into flip-flop circuits only on the positive going excursion of the clock or transfer line. When the clock is in either the binary 1 or binary 0 state, the data line (control input) may have large noise signals (up to 30v) without entering data into the flip-flop. Outputs on the "I" series line of modules are buffered, providing high-drive capability and noise rejection for signals on circuit outputs.

RELIABILITY All IC flatpacks are mounted on the printed circuit board with parallel gap soldering. This advanced technique for interconnecting integrated circuits offers the following advantages:

1) Circuits have mechanical strength without encapsulation.
2) Units may be removed and replaced with conventional soldering equipment.
3) Common problems associated with welding caused by slight variations in conductor width, plating thickness and lead size are eliminated.

Parallel gap soldering is basically a resistance soldering method but differs from conventional soldering in these respects:

a) No flux is used.
b) No solder is added.
c) Resistance welding equipment is used.
d) Parallel gap soldered joints are smaller than hand-soldered joints, can be made as fast as parallel gap welded joints and are made without subjecting the integrated circuit to any appreciable temperature rise. Consequently, units are repairable without damage to the printed circuit etch.

Circuit outputs are buffered with a drive transistor. If the output is accidentally damaged, it may be repaired simply by replacing the transistor instead of replacing the entire flat pack. Any output in the "I" series line may be shorted to ground without circuit damage.

NEW IC DIGITAL MODULES

IDC1	Decade counter with one digit decoder and 10 line output
IFF1	Flip-flop, 4 circuits, universal
IFF2	Flip-flop, 12 circuits, buffer storage, parallel in, parallel out
ISR1	Shift Register, 8-bit and 4-bit Serial in, Serial or Parallel out T & F out of each Flip-flop
ISR2	Shift Register, 16-bit Parallel or Serial in, Serial out, Parallel out for last 8-bits
ISR3	Shift Register, two 4-bit Serial or Parallel in, Serial or Parallel out T & F out of each FF
ISR4	Shift Register, two 14-bit Reg A Serial or Parallel in, Serial out Reg B Serial in or Parallel transfer from Reg A, Serial out

GENERAL SPECIFICATIONS

Frequency	DC to 200 KC
Logic Levels:	
One (−10v nominal)	−8 volts to −12 volts
Zero (0v. nominal)	+0.5 volts to −0.5 volts
Noise Rejection	
Clock Input	3.0 volts typical 1.5 volts guaranteed (under worst case temperature and load conditions)
Control Input	+2 volts to −30 volts (positive noise clamped at +2 volts)
Circuit Output	+3 volts to −3 volts
Operating Temperature	0°C to +55°C
Storage Temperature	−55°C to +125°C
Power Supply Voltages	

Raytheon Computer Integrated Circuit Modules

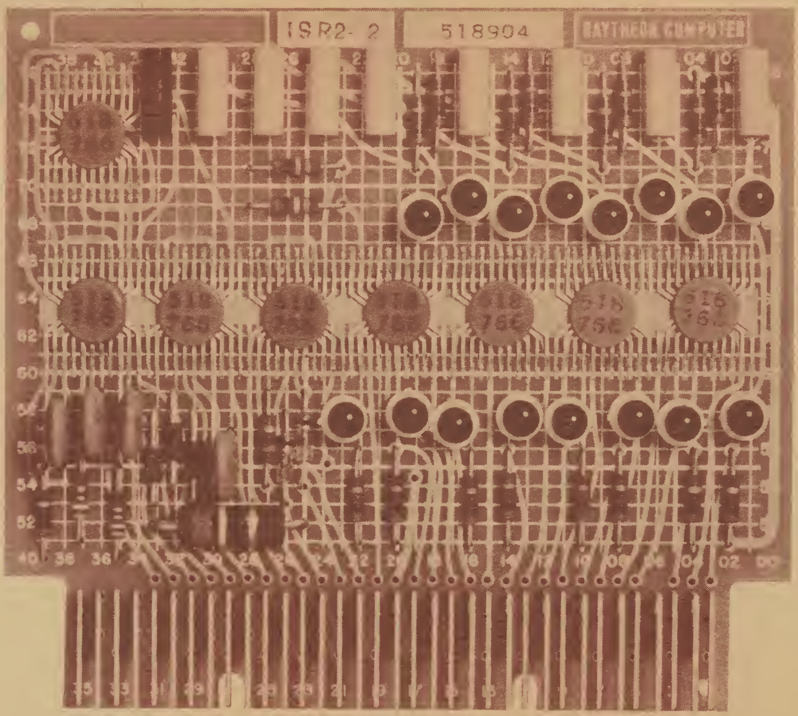
Superior Design Features

Unique Grid-Screen arrangement for component identification.

High Density—up to 28 flip-flops per card.

Color-coded test points on outputs for ease of system checkout

Decoupling on power input to reduce noise problems



(MODULE SHOWN ACTUAL SIZE)

Epoxy fiberglass board NEMA grade G-10 per MIL-E-16400E

35-pin Varicon connectors for density and reliability

Five-year Warranty

All boards keyed to insure proper installation

TRIGGER REQUIREMENTS Data is entered into the integrated circuit flip-flops when the clock or trigger input makes the transition from binary 1 to binary 0. The data that is entered into the flip-flop depends on the level of the control inputs immediately prior to the positive going transition of the clock or trigger input. When the set (J) input is binary 1 and the reset (K) input is binary 0, a clock signal will cause the set output to go to binary 1. When the reset input is binary 1 and the set input is binary 0, a signal on the clock input will cause the set output to go to binary 0. When both set and reset inputs are at binary 1, a clock signal will cause the flip-flop to toggle. This is due to the internal J-K steering which completely eliminates any ambiguity. When both set and reset inputs are at binary 0, no information can be entered into the flip-flop. The "I" series Flip-Flops are triggered identically to the "G" series flip-flops with one exception. In the "G" series flip-flops, if the toggle or clock input is at binary 1, a positive going signal on the data lines will cause information to be entered into the flip-flop. In the "I" series line, the control inputs are used for enabling or disabling only. Information is entered only on the positive going excursion of the clock or trigger input.

COMPONENT IDENTIFICATION Unique screen grid arrangement identifies components by number and position on the board. The grid contains numbers from 0 to 40 horizontally and from 50 to 76 vertically. A resistor labeled "R3068" would be located at the grid intersection of 30 and 68. This also locates the component on the horizontal plane or on the vertical plane. Components mounted on the vertical plane have the horizontal number first and are identified by the upper most lead. Components mounted on the horizontal plane have the vertical number first and are identified by the left most lead.

The grid technique allows a single identification screen to be used for all circuits.

Since parts lists also identify component location, they can be used instead of assembly drawings.

RAYTHEON COMPUTER
INTEGRATED CIRCUIT DIGITAL MODULES

RAYTHEON

IFF1 UNIVERSAL FLIP-FLOP

DESCRIPTION OF OPERATION

The IFF1 contains four Flip-flops for universal application. Each Flip-flop has internal J-K steering to eliminate ambiguity and counting or control. This circuit may be used as a decade counter, binary counter, parallel to serial or serial to parallel shift register, shift right shift left register or for general control applications.

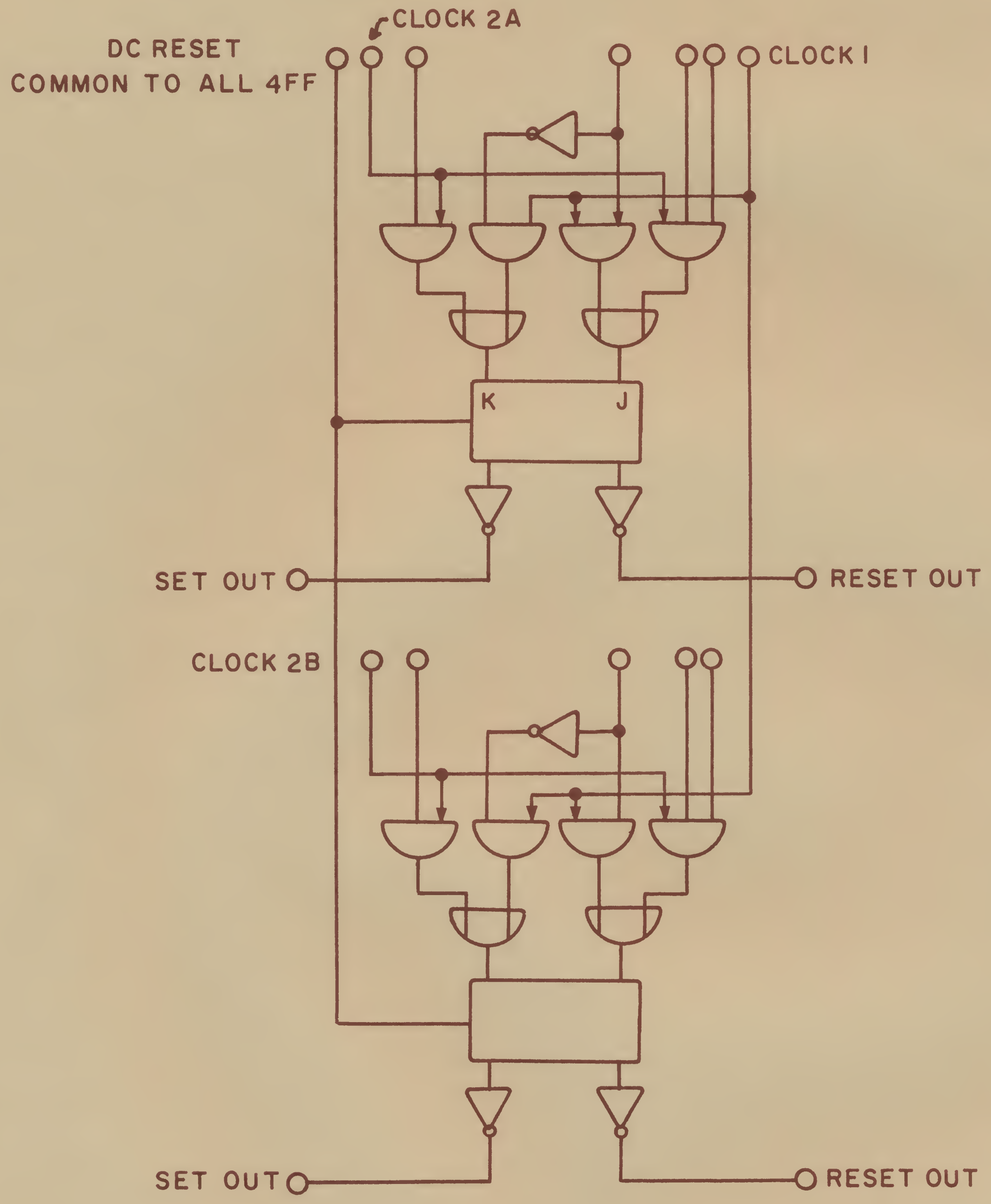
A "1" is entered into the flip-flop only when the control input is at binary "1" and the associated clock input goes from binary "1" to binary 0. Whether the clock inputs are at binary "1" or at binary "0", changed in the control inputs will not cause data to be entered into the flip-flop. When entering data via either clock input, the other clock input must be at binary "0".

The common reset input is a master DC reset that will cause the true (set) output of all flip-flops to go to the binary "0" state whenever the reset input is in the binary "1" state. The reset input should be at binary "0" for normal operation.

Any output may be shorted to ground without damage to the circuit. The circuits are essentially impervious to noise pulses on the output.

SPECIFICATIONS

MODULE	200 KC
FLIP-FLOP	IFF1
INPUT	
Frequency	0 to 200 KC
Voltage Levels	
One (-10V nominal)	-9 to -12V
Zero (0V nominal)	1 to -0.5V
Maximum Rise Time	1 μsec (for 200 KC operation)
Minimum dwell at binary one level	2 μsec
Input Load	
Resistive (per input pin)	5 megohms to ground (0.07 P loads)
Capacitive (per input pin)	10 pf
Noise Rejection	1.5V
OUTPUT	
Voltage Levels (full load)	
One (-10V nominal)	-9 to -12V
Zero (0V nominal)	0 to -0.3V
Maximum Rise Time (no load)	0.25 μsec
Maximum Fall Time (no load)	0.50 μsec
Maximum Rise Time (full load)	1 μsec
Drive Capability	10 N loads 7 P loads 2 C2 loads (at 200 KC) 4 C2 loads (at 100 KC for 5N loads maximum)
Maximum wiring capacitance per output	800 pf
PROPAGATION DELAY	
From 10% of Shift or Transfer input transition to 10% of output transition	0.6 μsec
POWER REQUIREMENTS per card	
-12V	110 ma
+6V	95 ma
-30V	.040 ma



IFF1 UNIVERSAL FLIP-FLOP

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RAYTHEON COMPUTER

INTEGRATED CIRCUIT DIGITAL MODULES

RAYTHEON

IFF2 BUFFER FLIP-FLOP

DESCRIPTION OF OPERATION

The IFF2 contains twelve (12) flip-flops in 3 groups of 4 flip-flops per group. This circuit is primarily for buffer storage. Each Flip-flop has a single input for jam transfer of data into the circuit. The set output of each flip-flop is available.

Each group of four flip-flops has a complement input. When a clock signal is applied to the complement input, all flip-flops in that group are complemented thus providing the 1's complement of the original data.

A "1" is entered into the flip-flop only when the control input is at binary "1" and the transfer input goes from binary "1" to binary "0". Whether the transfer input is at binary "1" or binary "0", changes in the control inputs will not cause data to be entered into the flip-flop. This is a jam transfer, thus, it is not necessary to clear the register prior to entering new data.

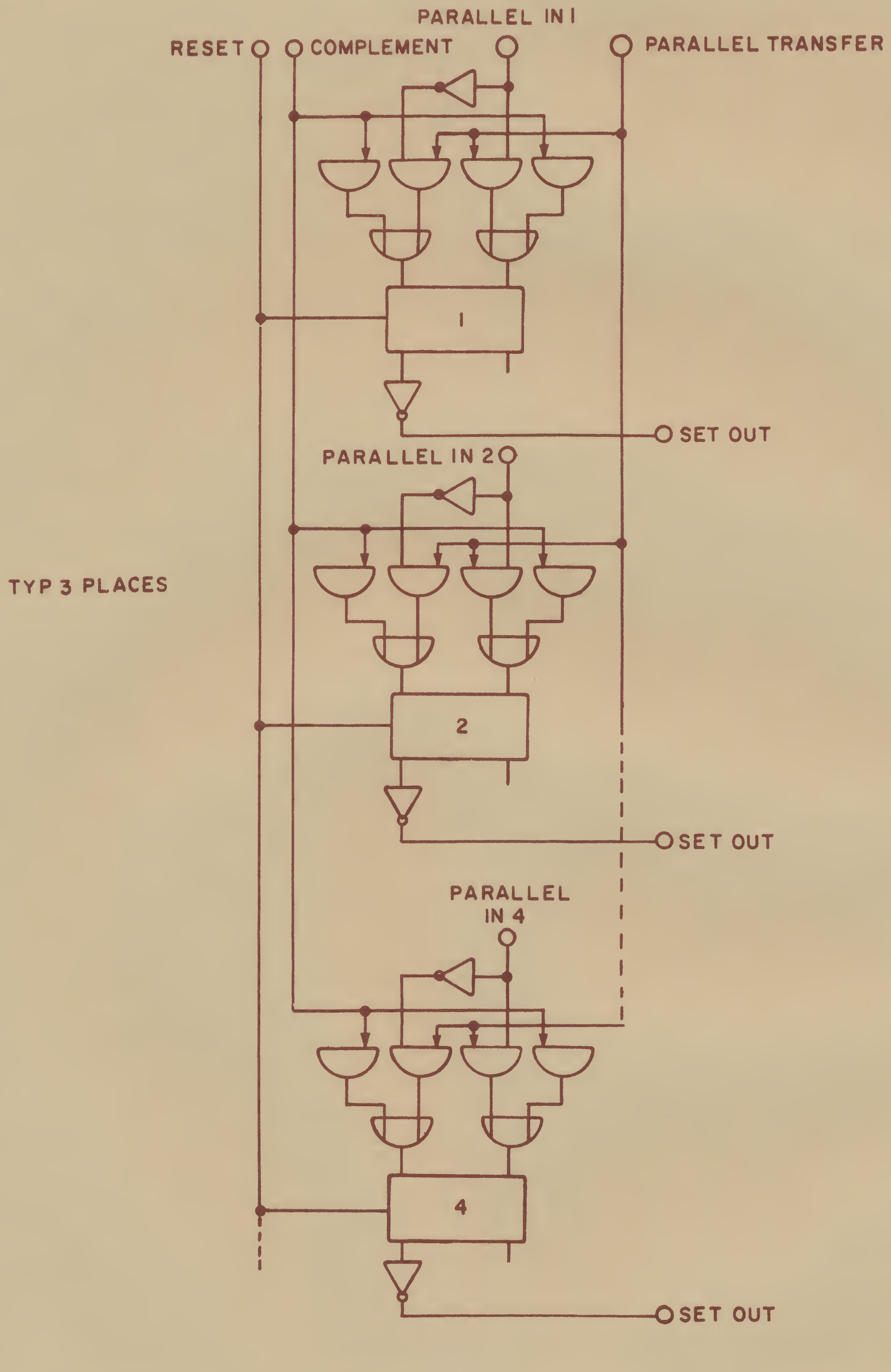
When entering data, the complement input should be at binary "0". When complementing the data, the transfer input should be at binary "0".

The common reset input is a master DC reset that will cause the true (set) output of all flip-flops to go to the binary "0" state whenever the reset input is in the binary "1" state. The reset input should be at binary "0" for normal operation.

Any output may be shorted to ground without damage to the circuit. The circuits are essentially impervious to noise pulses on the output.

SPECIFICATIONS

MODULE	200 KC
FLIP-FLOP	IFF2
INPUT	
Frequency	0 to 200 KC
Voltage Levels	
One (-10V nominal)	-9 to -12V
Zero (OV nominal)	0 to -0.5V
Maximum rise time	1 microsecond (for 200 KC operation)
Minimum dwell at binary one level	2 microseconds
Input Load	
Resistive (per input pin)	5 megohms to GND (0.07 P loads)
Capacitive (per input pin)	10 pf
Transfer clock input load	2 megohms and 20 pf to ground
Noise Rejection	
OUTPUT	
Voltage Levels (full load)	
One (-10V nominal)	-9 to -12V
Zero (OV nominal)	0 to -0.3V
Maximum rise time (no load)	0.25 microsecond
Maximum fall time (no Load)	0.50 microsecond
Maximum rise time (full load)	1 microsecond
Drive Capability; Set and Reset Outputs	10 N Loads 7 P Loads 2 C2 Loads (at 200 KC) 4 C2 Loads (at 100 KC for 5N loads max.)
Maximum wiring capacitance per output	800 pf
PROPAGATION DELAY	
From 10% of transfer input transition to 10% of output transition	0.6 microsecond
POWER REQUIREMENTS per card	
-12V	292 ma
+6V	155 ma
-30V	.12 ma



IFF2 BUFFER FLIP-FLOP

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INTEGRATED CIRCUIT DIGITAL MODULES

RAYTHEON

IDC1 DECADE COUNTER

DESCRIPTION OF OPERATION

The IDC1 contains four Flip-flops connected as a decade counter with decoding to provide ten lines output.

Each decade has a preset input for each Flip-flop. A "1" is entered into the Flip-flop when the preset input is at binary "1" (-10 v.) and the preset transfer input goes from binary "1" to binary "0". The preset input is a jam transfer, thus, it is not necessary to clear the counter prior to entering new data. The preset inputs are control inputs only. Whether the preset transfer input is at binary "1" or binary "0", changes in the preset inputs will not cause data to be entered into the flip-flop.

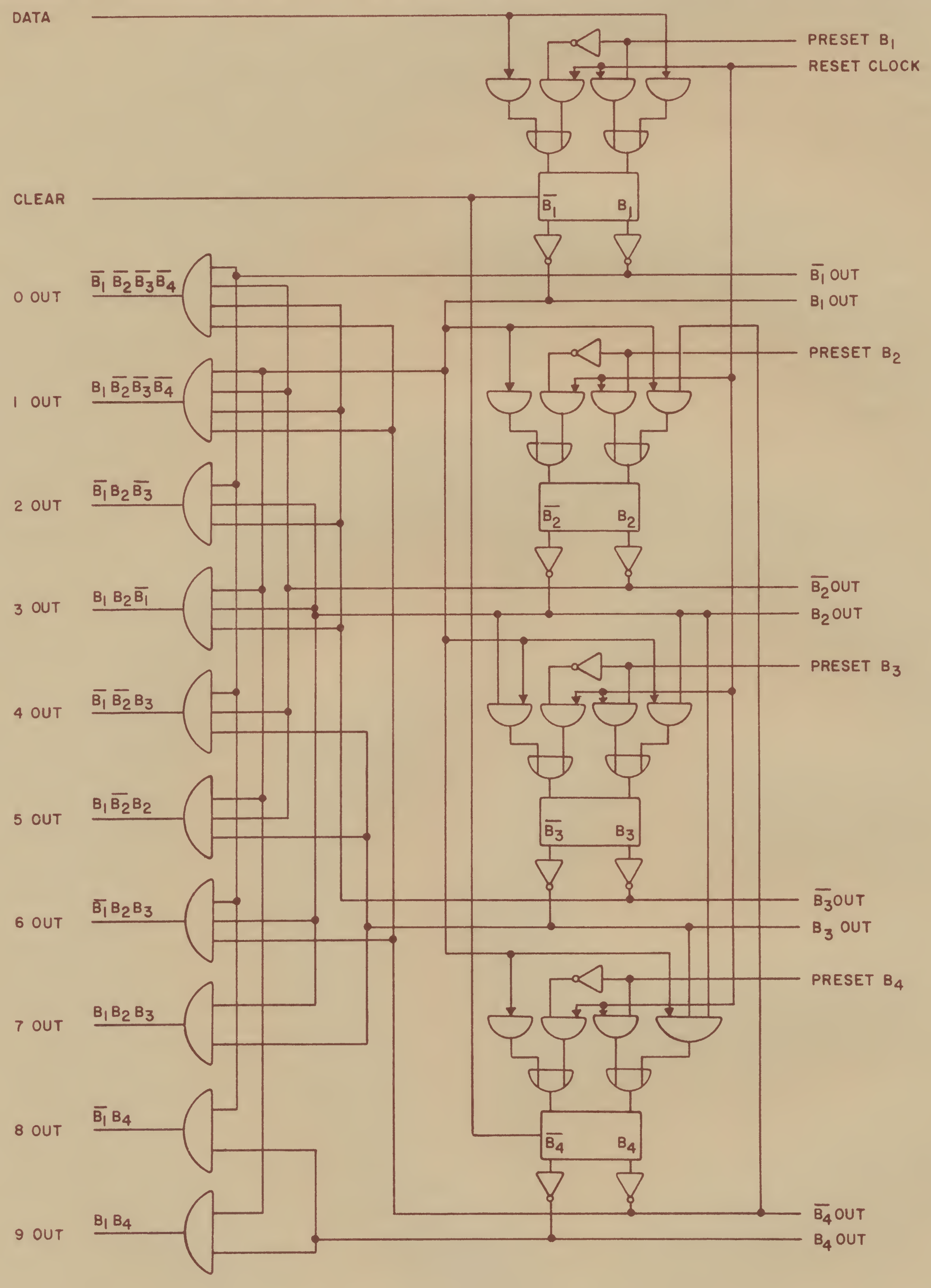
When entering preset data, the counter input should be at binary "0". When counting, the preset transfer input should be at binary "0".

The common reset input is a master DC reset that will cause the true (set) output of all flip-flops to go to the binary "0" state whenever the common reset input is in the binary "1" state. The common reset input should be at binary "0" for normal operation.

Any output may be shorted to ground without damage to the circuit. The circuits are essentially impervious to noise pulses on the output.

SPECIFICATIONS

MODULE	200 KC
FLIP-FLOP	IDC1
INPUT	
Frequency	0 to 200 KC
Voltage Levels	
One (-10V nominal)	-9 to -12V
Zero (0V nominal)	1 to -0.5V
Maximum Rise Time	1 μsec (for 200 KC operation)
Minimum dwell at binary one level	2 μsec
Input Load	
Resistive (per input pin)	5 megohms to ground (0.07 P loads)
Capacitive (per input pin)	10 pf
Preset transfer input load	1 megohm to gnd (0.35 P loads) and 12 pf
Noise Rejection	1.5V
OUTPUT	
Voltage Levels (full load)	
One (-10V nominal)	-9 to -12V
Zero (0V nominal)	0 to -0.3V
Maximum Rise Time (no load)	0.25 μsec
Maximum Fall Time (no load)	0.50 μsec
Maximum Rise Time (full load)	1 μsec
Drive Capability	10 N loads 7 P loads 2 C2 loads (at 200 KC); 4 C2 loads (at 100 KC for 5N loads maximum)
Maximum wiring capacitance per output	800 pf
PROPAGATION DELAY	
From 10% of the count input transition to 10% of the 4th Flip-Flop output transition	1.2 μsec
POWER REQUIREMENTS per card	
-12V	110 ma
+6V	95 ma
-30V	.040 ma



IDC1 DECADE COUNTER

RAYTHEON COMPUTER

INTEGRATED CIRCUIT DIGITAL MODULES

RAYTHEON

IUC1 UNIVERSAL COUNTER

DESCRIPTION OF OPERATION

The IUC1 contains 8 flip-flops which may be used as 2 independent decade counters or 2 4 bit binary counters. The counter may be made to count in either binary or decimal by wiring a single pin to either binary "1" (-12v) or binary "0" (0v) respectively. This input may also be controlled by external logic. Both binary and decimal counters count in the standard 8-4-2-1 code.

All flip-flops have preset capability. A "1" is entered into the flip-flop when the preset input is at binary "1" and the preset transfer input goes from binary "1" to binary "0". The preset input is a jam transfer thus it is not necessary to clear the counter prior to entering data. The preset inpus are control inputs only. Whether the preset transfer input is at binary "1" or binary "0", changes in the preset inputs will not cause data to be entered into the flip-flop.

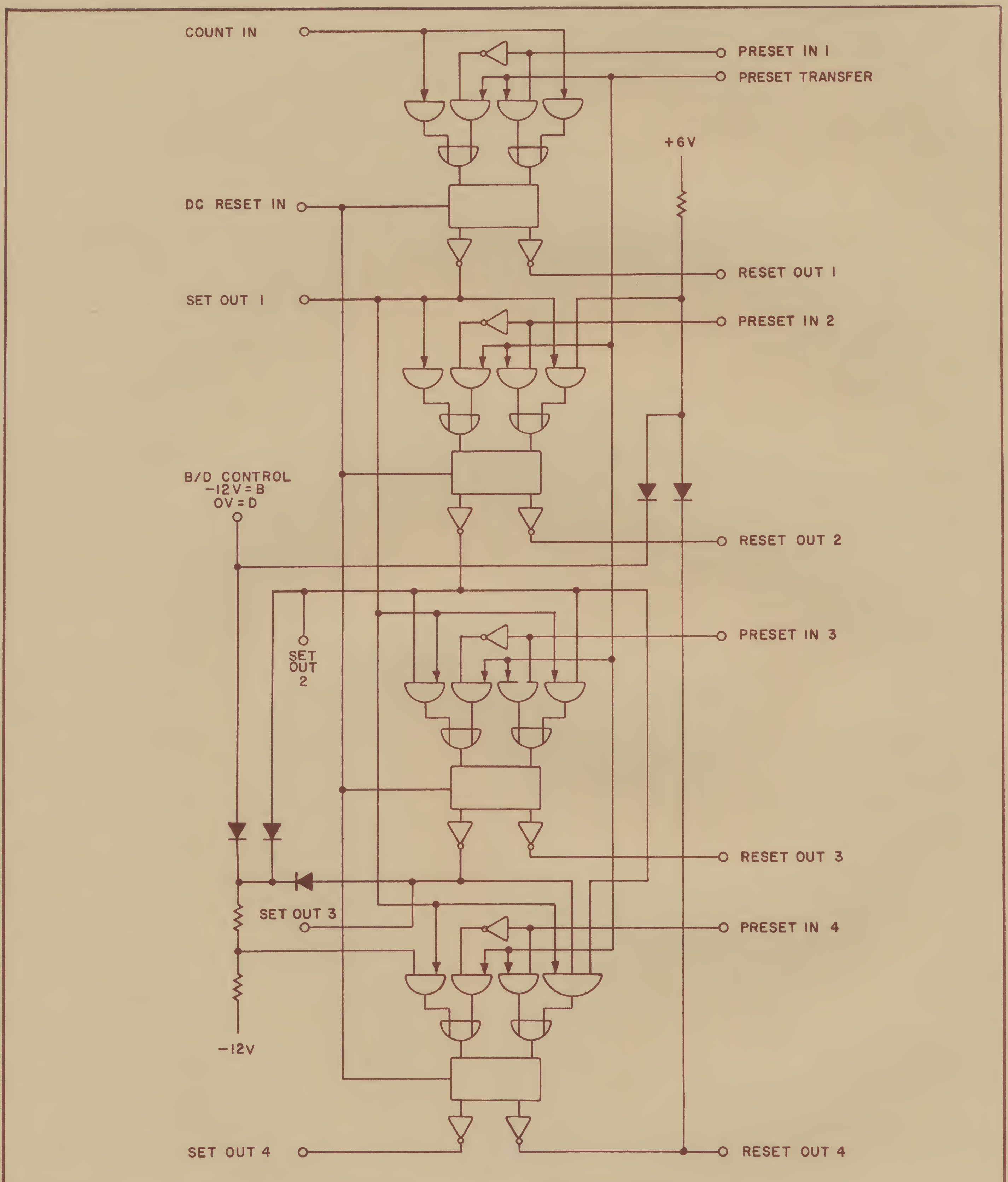
When entering preset data, the counter input should be at binary "0". When counting,the preset transfer input should be at binary "0".

The common reset input is a master DC reset that will cause the true (set) output of all flip-flops to go to the binary "0" state whenever the common reset input is in the binary "1" state. The common reset input should be at binary "0" for normal operation.

Any output may be shorted to ground without damage to the circuit. The circuits are essentially impervious to noise pulses on the output.

SPECIFICATIONS

MODULE	200 KC
INPUT	
Frequency	0 to 200 KC
Voltage Levels	
One (-10V nominal)	-9 to -12V
Zero (0V nominal)	0 to -0.5V
Maximum rise time	1 microsecond (for 200 KC operation)
Minimum dwell at binary one level	2 microseconds
INPUT LOAD	
Resistive (count, preset)	5 megohm to ground (0.07 P loads)
Capacitive (count, preset)	10 pf
B/D Control	0.5 N load
Noise Rejection	1.5V
OUTPUT	
Voltage Levels (full load)	
One (-10V nominal)	-9 to -12V
Zero (0V nominal)	0 to -0.3V
Maximum rise time (no load)	0.25 microsecond
Maximum fall time (no load)	0.50 microsecond
Maximum rise time (full load)	1 microsecond
Drive Capability	10 N loads 7 P loads 2 C2 loads (at 200 KC) 4 C2 loads (at 100 KC for 5 N loads max.)
Maximum wiring capacitance per output	800 pf
PROPAGATION DELAY	
From 10% of count input transition to 10% of last flip-flop output transition	1.2 microsecond
POWER REQUIREMENTS per card	
-12V	195 ma
+6V	125 ma
-30V	0.080 ma



IUC1 UNIVERSAL COUNTER

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2700 SOUTH FAIRVIEW ST., SANTA ANA, CALIFORNIA 92704

RAYTHEON COMPUTER

INTEGRATED CIRCUIT DIGITAL MODULES

RAYTHEON

ISR1 8-BIT AND 4-BIT SHIFT REGISTER

DESCRIPTION OF OPERATION

The ISR1 contains 12 Shift Register Flip-flops prewired as an 8 bit and a 4 bit serial to parallel registers. True and False outputs from each flip-flop are available and buffered to provide high drive capabilities. The Shift Input for the 8 bit register is driven through a 2 input AND gate. The node of the AND gate is available for expansion. The Shift Input for the 4 bit register is not gated. This may be gated externally, or to make a 12 bit serial to parallel Shift Register, connect the Shift Input for the 4 bit register to the gate node of the 8 bit and the True output of the 8th bit of the 8 bit register to the serial input of the 4 bit register. The serial input of both the 8 bit and the 4 bit have integral inverters so that only one input for each is required.

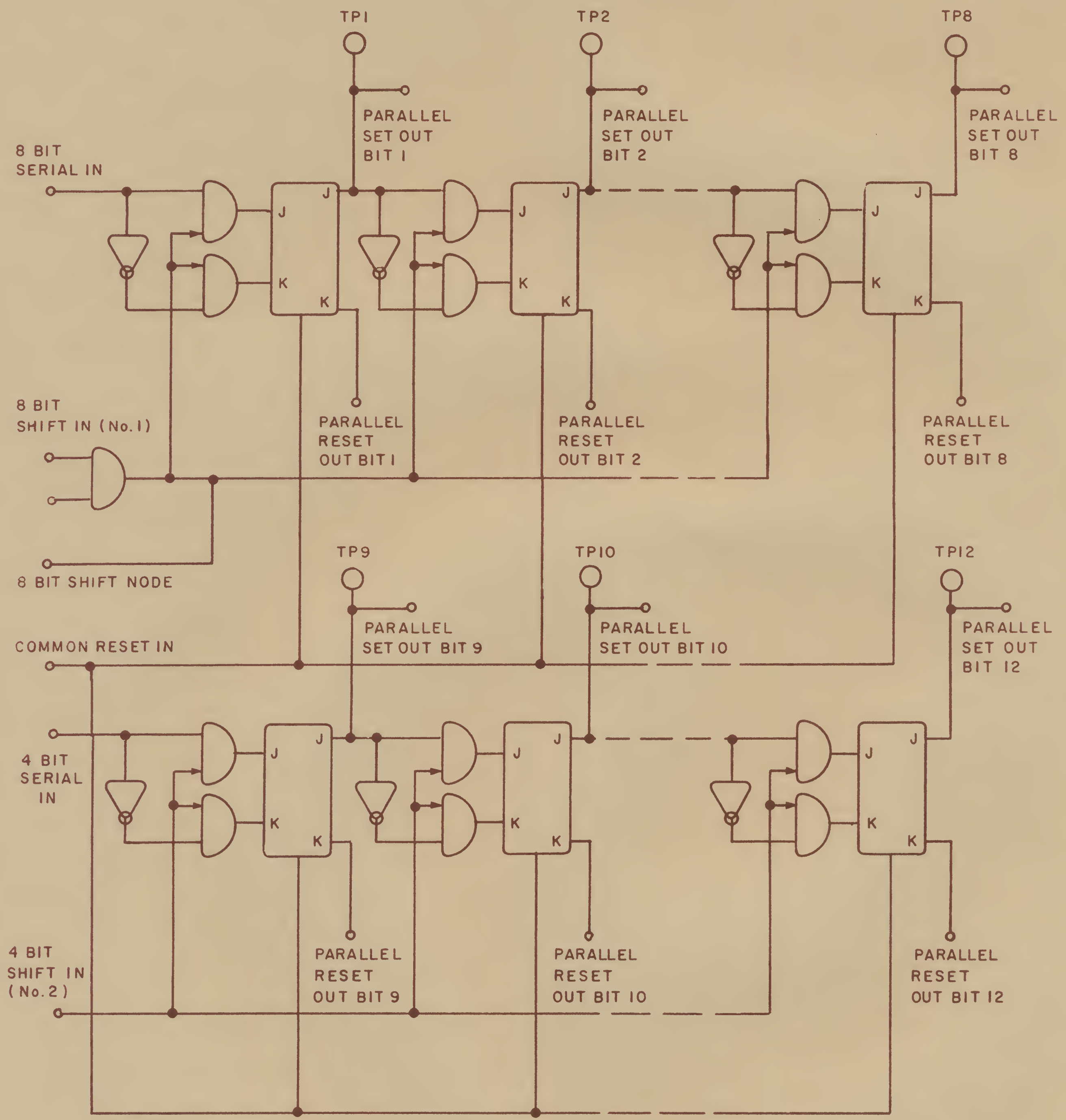
A "1" is entered into the register when the serial input is at binary "1" (-10 v.) and the Shift Input goes from binary "1" to binary "0" (0 v). The serial input is a control input only. Whether the Shift input is at binary "1" or binary "0", change in the serial input will not cause data to be entered into the register.

The common reset input is a master DC reset that will cause the True output of all Flip-flops to go to the binary "0" state whenever the reset input is in the binary "1" state. The reset input should be at binary "0" for normal operation.

Any output may be shorted to ground without damage to the circuit. The circuits are essentially impervious to noise pulses on the output.

SPECIFICATIONS

MODULE	200 Kc.
SHIFT REGISTER	ISR1
INPUT	
Frequency	0 to 200 Kc.
Voltage Levels	
One (-10V nominal)	-9 to -12V
Zero (0V nominal)	+1 to -0.5V
Shift inputs, Reset input, and Serial inputs	
Max. rise time	1 μsec (for 200 Kc operation)
Min. dwell at binary one level	2 μsec
Shift #2, Reset, and Serial input load to gnd.	0.1 P Load (1 Meg Ω)
Shift #1 input load	1 N load
Noise Rejection	1.5 V
OUTPUT	
Voltage Levels (full load)	
One (-10V nominal)	-9 to -12V
Zero (0V nominal)	0 to -0.3V
Maximum rise time (no load)	0.25 μsec
Maximum fall time (no load)	0.50 μsec
Maximum rise time (full load)	1 μsec
Drive Capability; Set & Reset Outputs	10 N loads 7 P loads 2 C2 loads (at 200 Kc) 4 C2 loads (at 100 Kc for 5 N loads max)
Maximum wiring capacitance per output	800 pf
PROPAGATION DELAY	
From 10% of Shift input transition to 10% of output transition (Full load).	0.6 μsec
POWER REQUIREMENTS per Card	
-12V	260 ma
+6V	145 ma
-30V	0.12 ma



ISR1 8-BIT AND 4-BIT SHIFT REGISTER

RAYTHEON COMPUTER

INTEGRATED CIRCUIT DIGITAL MODULES

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ISR2 16-BIT SHIFT REGISTER

DESCRIPTION OF OPERATION

The ISR2 contains 16 Shift Register Flip-flops prewired as a parallel to serial register. The ISR2 can also be used as a 16 bit serial to serial Shift Register.

A "1" is entered into the register when the parallel data input is at binary "1" (-10 v) and the parallel transfer input goes from binary "1" to binary "0". The parallel entry is a jam transfer thus it is not necessary to clear the register prior to entering new data.

When entering parallel data, the Shift Input should be at binary "0". When shifting data, the parallel transfer input should be at binary "0".

The Shift Input is driven through a 2 input AND gate. The data is shifted serially one bit each time the Shift Input goes from binary "1" to binary "0". If the serial input is not used, the Register will automatically enter a "0" with each shift pulse.

The parallel data entry and serial data entry are control inputs only. Whether the Shift or Transfer inputs are at binary "1" or binary "0", changes in the control inputs will not cause data to be entered into the register.

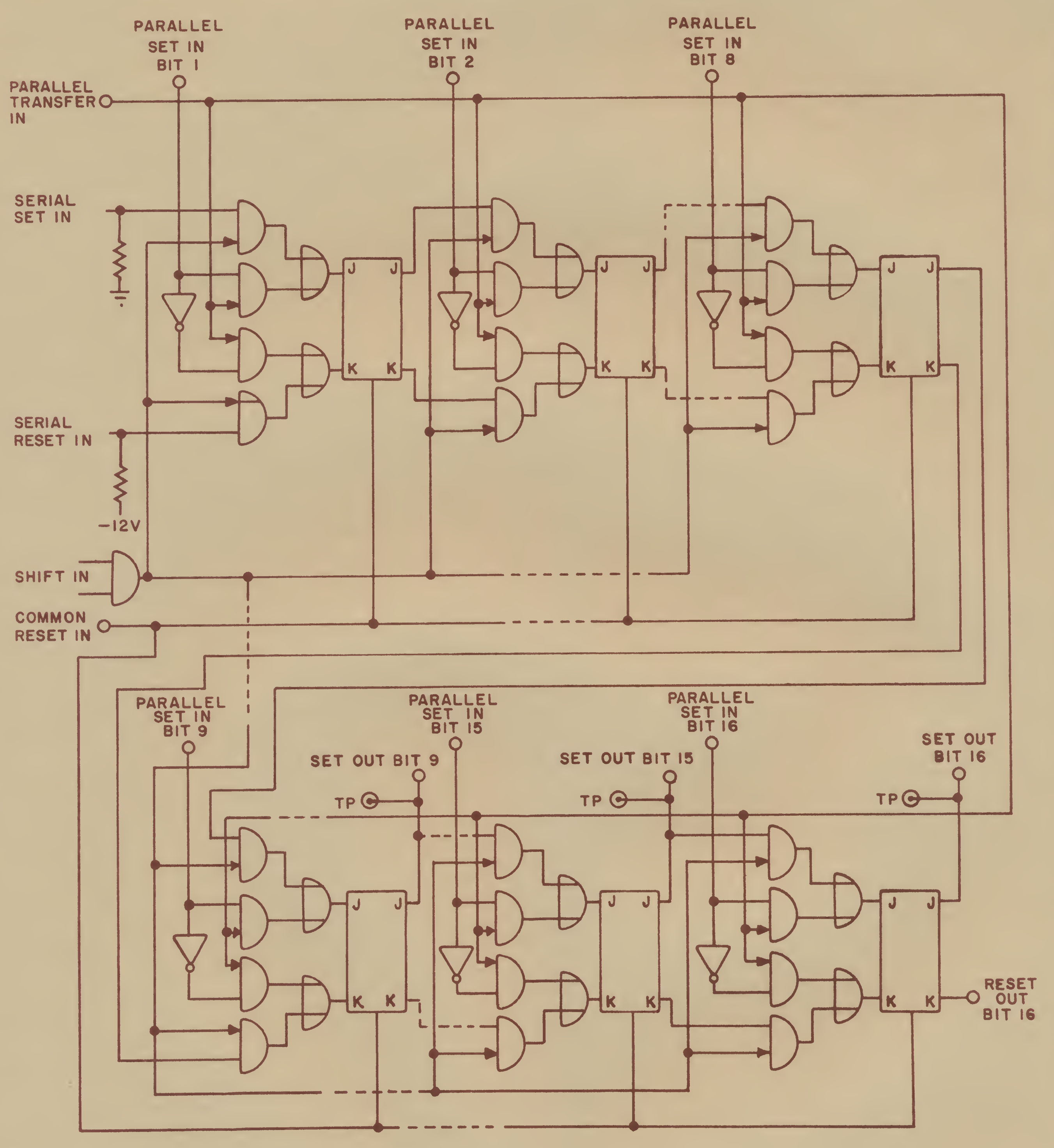
Bits 9 through 16 have the True output available. The 16th bit has both True and False outputs available. All outputs are buffered for high drive capability.

The common reset input is a master DC reset that will cause the True output of all Flip-flops to go to the binary "0" state whenever the reset input is in the binary "1" state. The reset input should be at binary "0" for normal operation.

Any output may be shorted to ground without damage to the circuit. The circuits are essentially impervious to noise pulses on the output.

SPECIFICATIONS

ISR2 16-BIT SHIFT REGISTER	200 Kc.
INPUT	
Frequency	0 to 200 Kc.
Voltage Levels	
One (-10V nominal)	-9 to -12V
Zero (0V nominal)	+1 to -0.5V
Shift & Transfer inputs, Reset input, serial inputs and parallel inputs	
Max. rise time	1 μsec (for 200 Kc operation)
Min. dwell at binary one level	2 μsec
Parallel transfer, Reset, and Parallel input load to gnd	0.1 P load (Meg Ω)
Shift pulse input load	1 N load
Serial input loads	
Set input	1/2 P load
Reset input	0.1 N load
Noise Rejection	1.5 V
OUTPUT	
Voltage Levels (full load)	
One (-10V nominal)	-9 to -12V
Zero (0V nominal)	0 to -0.3V
Maximum rise time (no load)	0.25 μsec
Maximum fall time (no load)	0.50 μsec
Maximum rise time (full load)	1 μsec
Driver Capability	10 N loads 7 P loads 2 C2 loads (at 200 Kc) 4 C2 loads (at 100 Kc for 5 N loads max)
Maximum wiring capacitance per output	800 pf
PROPAGATION DELAY	
From 10% of Shift or Transfer input transition to 10% of output transition (Full load)	0.6 μsec
POWER REQUIREMENTS per Card	
-12V	240 ma
+6V	185 ma
-30V	0.16 ma



ISR2 16-BIT SHIFT REGISTER

RAYTHEON COMPUTER
2700 SOUTH FAIRVIEW ST., SANTA ANA, CALIFORNIA 92704

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ISR3 DUAL 4-BIT UNIVERSAL SHIFT REGISTER

DESCRIPTION OF OPERATION

The ISR3 contains 8 Universal Registers in two groups of four. Each group is suitable for serial to parallel, parallel to parallel or serial to serial operation.

A single input is required for each stage for either parallel entry or serial shifting. An integral Inverter is included on each stage eliminating the need for both True and False inputs.

For serial operation, connect the True output of each stage to the input of the following stage: each 4 stage register has a separate gated Shift or transfer input. Data is transferred into the register or shifted one bit when the shift/transfer goes from binary "1" to binary "0".

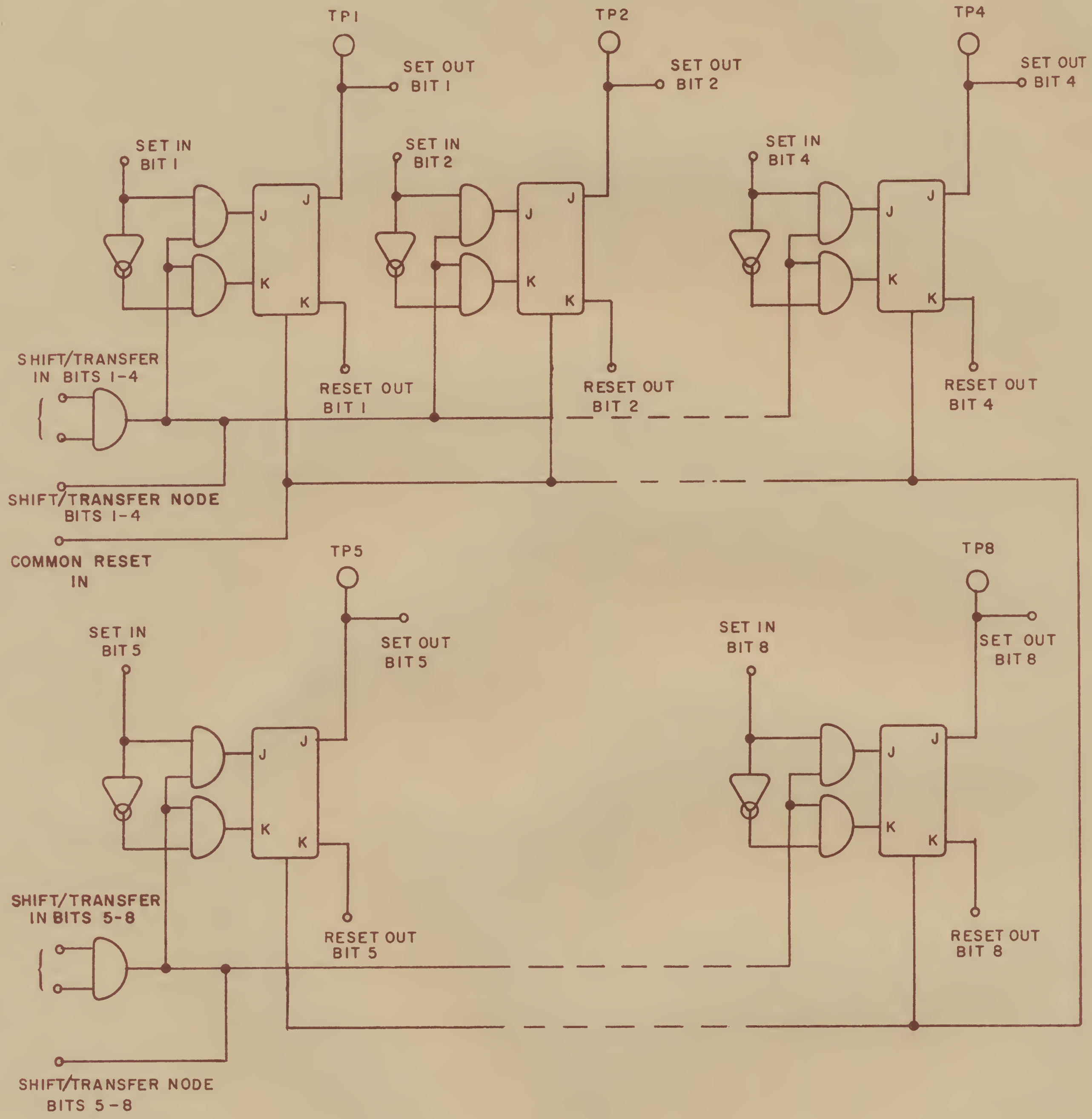
All outputs are buffered for high drive capability.

The common reset input is a master DC reset that will cause the True output of the Flip-flops to go to the binary "0" state whenever the reset input is in the binary "1" state. The reset input should be at binary "0" for normal operation.

Any output may be shorted to ground without damage to the circuit. The circuits are essentially impervious to noise pulses on the output.

SPECIFICATIONS

MODULE	200 Kc.
SHIFT REGISTER	ISR3
INPUT	
Frequency	0 to 200 Kc.
Voltage Levels	
One (-10V nominal)	-9 to -12V
Zero (0V nominal)	0 to -0.5V
Shift or Transfer inputs, serial, parallel, and reset inputs	
Max. rise time	1 μsec (for 200 Kc operation)
Min. dwell at binary one level	2 μsec
Shift/Transfer input load	1 N load
Serial, parallel, or reset input load to gnd.	0.1 P load (1 Meg Ω).
Noise Rejection	1.5V
OUTPUT	
Voltage Levels (full load)	
One (-10V nominal)	-9 to -12V
Zero (0V nominal)	0 to -0.3V
Maximum rise time (no load)	0.25 μsec
Maximum fall time (no load)	0.50 μsec
Maximum rise time (full load)	1 μsec
Drive Capability Set & Reset Outputs	10 N loads 7 P loads 2 C2 loads (at 200 Kc) 4 C2 loads (at 100 Kc for 5 N loads max)
Maximum wiring capacitance per output	800 pf
PROPAGATION DELAY	
From 10% of Shift or Transfer input transition to 10% of output transition (full load)	0.6 μsec
POWER REQUIREMENTS per Card	
-12V	180 ma
+6V	105 ma
-30V	0.080 ma



ISR3 DUAL 4-BIT UNIVERSAL SHIFT REGISTER

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INTEGRATED CIRCUIT DIGITAL MODULES

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ISR4

DESCRIPTION OF OPERATION

The ISR4 contains 28 shift register flip-flops. Each flip-flop has internal J-K stearing to eliminate ambiguity in shifting or data control. The 28 flip-flops are broken into two registers of 14-bit capability each. The "A" register is capable of receiving external data in either a serial or parallel manner. The "B" register may receive 14-bit parallel data from the "A" register by means of jam transfer or data from an external source or the "A" register in a serial manner.

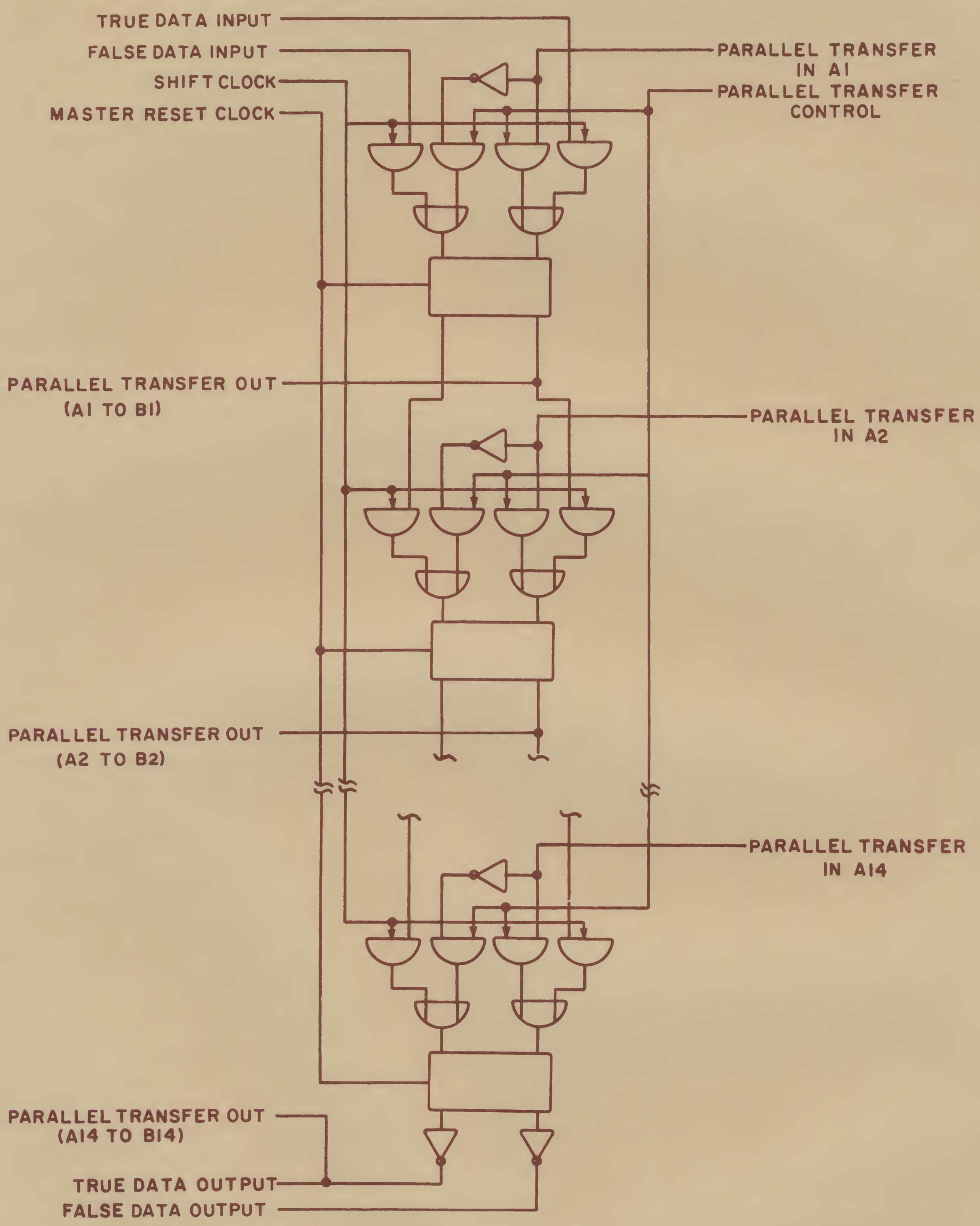
A "1" is entered into the register only when the control input is at binary "1" and the associated clock input goes from binary "1" to binary "0". Whether the clock inputs are at binary "1" or at binary "0", changes in the control inputs will not cause data to be entered into the register. When entering data via either clock input, the other clock input must be at binary "0".

The common reset input is a master DC reset that will cause the true (set) output of both registers to go to the binary "0" state whenever the reset input is in the binary "1" state. The reset input should be at binary "0" for normal operation.

The serial output, the fourteenth and twenty-eighth flip-flops, contain both true and false buffered output for stored data access. These output may be shorted to ground without circuit damage and are virtually impervious to noise

SPECIFICATIONS

MODULE	200 KC
SHIFT REGISTER	ISR4
INPUT	
Frequency	0 to 200 KC
Voltage Levels	
One (-10V nominal)	-9 to -12V
Zero (0V nominal)	1 to -0.5V
Maximum rise time	1 microsecond (for 200 KC operation)
Minimum dwell at binary one level	2 microseconds
Input Load	
Resistive (per input pin)	5 megohms to ground (0.07 P loads)
Capacitive (per input pin)	10 pf
Clock Input Load (per register)	
Resistive Load	320 K ohms
Capacitance	50 pf
Noise Rejection	1.5V
OUTPUT	
Voltage Levels (full load)	
One (-10V nominal)	-9 to -12V
Zero (0V nominal)	0 to -0.3V
Maximum Rise Time (no load)	0.25 microsecond
Maximum Fall Time (no load)	0.50 microsecond
Maximum Rise Time (full load)	1 microsecond
Drive Capability	10 N loads 7 P loads 2 C2 loads (at 200 KC) 4 C2 loads (at 100 KC for 5N loads max.)
Maximum wiring capacitance per output	800 pf
PROPAGATION DELAY	
From 10% of shift or transfer input transition to 10% of output transition	0.6 microsecond
POWER REQUIREMENTS per card	
-12V	500 ma
+6V	485 ma
-30V	.280 ma


TRUE DATA INPUT
FALSE DATA INPUT
SHIFT CLOCK
MASTER RESET CLOCK
PARALLEL TRANSFER IN A1
PARALLEL TRANSFER CONTROL
PARALLEL TRANSFER OUT (A1 TO B1)
PARALLEL TRANSFER IN A2
PARALLEL TRANSFER OUT (A2 TO B2)
PARALLEL TRANSFER IN A14
PARALLEL TRANSFER OUT (A14 TO B14)
TRUE DATA OUTPUT
FALSE DATA OUTPUT

ISR4

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INTEGRATED CIRCUIT DIGITAL MODULES

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ISR5

DESCRIPTION OF OPERATION

The ISR5 contains 24 shift register flip-flops. Each flip-flop has internal J-K steering to eliminate ambiguity in shifting or data control. The 24 flip-flops are broken into two registers of 12-bit capability each. The "A" register is capable of receiving external data in either a serial or parallel manner. The "B" register may receive 12-bit parallel data from the "A" register by means of jam transfer or data from an external source or the "A" register in a serial manner.

A "1" is entered into the register only when the control input is at binary "1" and the associated clock input goes from binary "1" to binary "0". Whether the clock inputs are at binary "1" or at binary "0", changes in the control inputs will not cause data to be entered into the register. When entering data via either clock input, the other clock input must be at binayr "0".

The common reset input is a master DC reset that will cause the true (set) output of both registers to go to the binary "0" state whenever the reset input is in the binary "1" state. The reset input should be at binary "0" for normal operation.

The twelfth and twentyfourth flip-flops, serial outputs, contain both true and false buffered output for stored data access. These outputs may be shorted to ground without circuit damage and are virtually impervious to noise.

SPECIFICATIONS

MODULE	200 KC
FLIP-FLOP	ISR5
INPUT	
Frequency	0 to 200 KC
Voltage Levels	
One (-10V nominal)	-9 to -12V
Zero (0V nominal)	1 to -0.5V
Maximum Rise Time	1 μsec (for 200 KC operation)
Minimum dwell at binary one level	2 μsec
Input Load	
Resistive (per input pin)	5 migohms to ground (0.07 P loads)
Capacitive (per input pin)	10 pf
Clock Input Load	
Resistive Load	380 K ohms
Capacitive Load	45 pf
Noise Rejection	1.5V
OUTPUT	
Voltage Levels (full load)	
One (-10V nominal)	-9 to -12V
Zero (0V nominal)	0 to -0.3V
Maximum Rise Time (no load)	0.25 μsec
Maximum Fall Time (no load)	0.50 μsec
Maximum Rise Time (full load)	1 μsec
Drive Capability	10 N loads 7 P loads 2 C2 loads (at 200 KC) 4 C2 loads (at 100 KC for 5N loads max.)
Maximum wiring capacitance per output	800 pf
PROPAGATION DELAY	
From 10% of Shift or Transfer Input Transition to 10% of Output Transition	0.6 μsec
POWER REQUIREMENTS per Card	
-12V	425 ma
+6V	425 ma
-30V	.240 ma

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INTEGRATED CIRCUIT MODULES - NOISE REJECTION

CLOCK LINE

The clock line is used to transfer data into the Flip-flop. When the clock signal makes the transition from binary "1" (-10 v) to binary "0" (0 v), data is entered into the Flip-flop. Whether the clock signal is at binary "1" or binary "0", noise pulses of +1.5 v or less, regardless of rise or fall time, will not cause data to be entered into the Flip-flop.

DATA LINE (CONTROL INPUT)

The value of the control input approximately 0.2 μs before the positive transition of the clock determines whether a "1" or a "0" is entered into the Flip-flop. The Raytheon Computer "1" Series modules have two types of control inputs:

1. Preset or Parallel Data Control - whether the clock signal is binary "1" or binary "0", the noise rejection for the Preset or Parallel data control line is 30 v at all times except for the period immediately prior to the positive transition of the clock, (approximately 0.2 μs). During this period, the clock is sampling the control inputs and the noise rejection is 1.5 v.

2. Separate Set and Reset control inputs - the noise rejection for the separate Set and Reset control inputs is 30 v at all times except when both inputs are binary "0" and the clock input is binary "1" or during the period immediately prior to the positive transition of the clock (approximately 0.2 μs). During these periods, the noise rejection is 1.5 v.

Positive noise transients on all inputs are clamped at +2 v. Steady state voltages more positive than +2 v or more negative than -15 v should not be applied to the input.

The noise rejection of 1.5 v is for all worst case conditions of load, temperature and ±10% power supply variation. Typical noise rejection is 3 v.

RAYTHEON COMPUTER

INTEGRATED CIRCUIT DIGITAL MODULES

PRICE LIST

IDC1	DECADE COUNTER	$	80.00
	One decimal digit with decoder and 10 line output. True and false outputs for all flip flops. Preset input into counter. Master reset.		
IFF1	FLIP-FLOP, UNIVERSAL		68.00
	4 gated J-K flip flops with true and false outputs. May be used as decade counter, serial or parallel shift register, shift right - shift left register or general control applications. Master reset.		
IFF2	FLIP-FLOP, BUFFER		168.00
	12 flip flops in 3 groups of 4 flip flops. Parallel in, parallel out. Serial in, parallel or serial out. True output for all flip flops. Complement input to generate One's complement. Master reset.		
ISR1	SHIFT REGISTER		170.00
	12 shift register flip flops serial to parallel. One 8-bit and one 4-bit. Gated shift input for the 8-bit register. True and false outputs for all flip flops. Master reset.		
ISR2	SHIFT REGISTER		186.00
	16-bit parallel to serial or serial to serial. True outputs for last 8 bits. Gated shift input. Master reset.		
ISR3	SHIFT REGISTER		119.00
	8 universal registers in two groups of four. Each group is suitable for serial to parallel, parallel to parallel, or serial to serial operation. Shift inputs are gated. True and false outputs for all flip flops. Master reset.		
ISR4	SHIFT REGISTER		318.00
	Two 14-bit registers parallel or serial into Register A. Serial out of Register A or parallel transfer from Register A to Register B. Serial in and out of Register B. Master reset.		
ISR5	SHIFT REGISTER		275.00
	Same as ISR 4 except 12-bit registers instead of 14-bit.		
IUC1	UNIVERSAL COUNTER		124.00
	8 flip flops which may be used as two independent decade counters or two 4-bit binary counters. True and false outputs from all flip flops. Preset input for all flip flops. Master reset.		
IPS1	POWER SUPPLY -30V		35.00
	Bias supply for integrated circuit flip flops. Mounted on standard board. Utilizes -12V and converts to -30V. Suitable for 300 flip flops.		

Sept. 1, 1965